RESUME

GOGIREDDY LEELAVATHI

Gmail: leelavathigogireddy@gmail.com
MobileNo:**6301973460**

Career Objective

Looking forward for a challenging position in a growing IT organization in which I can find simple opportunities form professional growth and best utilizes technical expertise, experience innovative abilities and interpersonal skills so that I can render increasingly effective services to the organization.

Professional Summery

- Well versed with **Core JAVA, HTML, MY SQL languages** and **advanced java.**
- Possess excellent interpersonal and communication skills and self-motivation.
- Good Aptitude and Problem-solving skills.
- Good ability to quickly and master new concepts and technologies.
- Having good Knowledge in Manual Testing.

Education Details

- Bachelor of Technology in the stream of Electronics and Communications Engineering from JNTUK in 2023with a CGPA of 7.69.
- Completed Intermediate in 2019 from vidya Bharathi junior college with CGPA of 9.65.
- Completed SSC in 2017 from zphs high school with CGPA of 8.0.

Technical Skills

Software languages: ☐**Core JAVA, HTML, MY SQL,**

In Advanced Java : JDBC, SERVLETS, JSP, HIBERNET, SPRING, SPRINGBOOT.

Experience:(One year)

Domain: software engineer

Company: Techzert software private limited

Job Description:

Worked on setting up, configuring, and supporting IBM API Connect environments in a VMware and Ubuntu Linux setup. Performed platform upgrades with proper pre- and post-upgrade validation to ensure system stability. Designed and developed REST APIs using Open API (Swagger 3.0) and integrated them with backend services using assembly policies. Managed API deployments across Dev, Test, and Production environments and ensured proper security implementation. Monitored logs, troubleshot errors, and tested APIs using Postman and apic tools to maintain smooth functionality.

Project

Name: TWO STEP LOW POWER HIGH SPEED CMOS FLASH ADC ARCHITECTURE.
Team Size: 4

Description: In my project, I am the team leader. The project aims to design in old design there are used large areas and many transistors and large amounts of power. but at low speed. That is why we are using this CMOS technology. We decrease the area and number of transistors and so decrease the time and use of power decreases, speed increases using this technology.

A-6-bit, 1.8 V two-step low power flash ADC has been designed, and the performance was analyzed with the conventional flash ADC. The architecture was implemented using 180 nm CMOS technology. The concept of MSB generation with a switched reference voltage was employed in the proposed flash ADC architecture to reduce the number of comparators; it requires only 2N−1 comparators. Further, in the present design, 658 CMOS transistors are available.

were used, whereas in conventional flash ADC 1392 CMOS transistors were used. In addition, a low power encoder has been designed for the proposed flash ADC. The ADC was operated at 1 MHz, and through simulation, it was found that the total power consumption was 604.28 µW.

My Responsibilities:

- Gathering the equipment and designing.
- Collecting the previous old model and comparing the old design and new design and identify the difference
  Which one is the better.

Personaldetails

- Name : G.Leelavathi
- Father Name : G.lachi reddy
- Date of Birth : 30/09/2002
- Nationality : Indian
- Gender : female
- Marital status : Single
- Languages Known: English, Telugu and Hindi(basic)
- Hobbies : watching movies, Listing to music.
- Address : pedagarla padu(village), Guntur(dist), Andhra Pradesh.

Declaration

I hereby declare that the above written particulars are true to the best of my knowledge and belief.

Date: 24/11/2025
G. LEELAVATHI